Performance of Dual-Gate GaAs MESFET's as Gain-Controlled Low-Noise Amplifiers and High-Speed Modulators

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Abstract—**This paper describes the microwave performance of GaAs FET's with two 1-μm Schottky-barrier gates (dual-gate MESFET). At 10 GHz the MESFET, with an inductive second-gate termination, exhibits an 18-dB gain with −26-dB reverse isolation. Variation of the second-gate potential yields a 44-dB gain-modulation range. The minimum noise figure is 4.0 dB with 12-dB associated gain at 10 GHz. Pulse modulation of an RF carrier with a 65-ps fall and a 100-ps rise time is demonstrated. The dual-gate MESFET with high gain and low noise figure is especially suited for receiver amplifiers with automatic gain control (AGC) as an option. The MESFET is equally attractive for subnanosecond pulsed-amplitude modulation (PAM), phase-shift-keyed (PSK), and frequency-shift-keyed (FSK) carrier modulation.**

I. INTRODUCTION

THE gallium arsenide field-effect transistor with Schottky-barrier gate (GaAs MESFET) is the next generation of small-signal low-noise transistors. Owing to the high electron mobility and high peak-drift-velocity in GaAs, the MESFET exhibits shorter transit times than silicon transistors. The useful frequency range is extended more than a factor of 2 over present bipolar transistors. The gain and noise performance of single-gate GaAs MESFET's have been extensively characterized [1]–[6], and the MESFET potential in low-noise amplifiers has been clearly demonstrated [7]–[16].

Another member in the MESFET family with very attractive gain and noise performance, stability, and modulation capabilities is the dual-gate MESFET. This transistor has two parallel gate electrodes between source and drain. The dual-gate MESFET is normally operated in common-source configuration. The RF input signal is applied between the first gate and the source. The output signal between drain and source is coupled to the load. The second gate is usually RF grounded. The superior stability of the dual-gate MESFET has been demonstrated [17], [18]. In addition, it has been shown that dc bias applied to the second gate varies the RF gain [17]–[22]. A negative bias beyond the pinch-off voltage yields a large insertion loss, and positive bias yields a gain maximum that is considerably higher than the gain of a single-gate device with equal dimensions. Many characteristics are qualitatively analogous to those of dual-gate Si MOSFET's used in UHF receivers [23]–[26]. Both MESFET's and MOSFET's have traditionally been characterized as two-port devices with the second gate RF grounded. A more general approach deals with the dual-gate MESFET as a three-port device [27]. If one connects an RF impedance between the second gate and source, then the properties of the resulting two-port can easily be expressed as functions of this impedance. It will be shown that this impedance has a strong influence on many MESFET parameters. With a proper choice, the gain or stability can be optimized or the noise measure minimized.

The purpose of this paper is to discuss the characteristics of the dual-gate MESFET as a high-gain low-noise amplifier with voltage-controlled gain and as a high-speed RF modulator. First, measured three-terminal s-parameters will be described, and the forward gain and reverse isolation will be computed for various impedances connected between the second gate and source. In addition, the gain versus frequency will be characterized. Second, the bias at the second gate will be varied, and the resulting gain, input impedance, and transmission-phase change will be discussed. Third, the noise performance and power capability will be compared with single-gate MESFET's. Fourth, the high-speed modulation capability will be demonstrated. A major objective is to show clearly the differences between the single-gate and the dual-gate MESFET performance. Realizing each FET version's unique features will lead, at the end of this paper, to obvious conclusions for their application.

II. DEVICE DESCRIPTION AND SIGNAL FLOW GRAPH

The MESFET is fabricated on a semi-insulating Cr-doped GaAs substrate that is covered with a thin n-type epitaxial layer. The conducting layer is grown from Sn-doped Ga solution on the ⟨100⟩ substrate face. The doping is 7×10^{16} cm^{-3}, and the layer thickness is 0.2 μm in the channel region. A microphotograph of the chip is shown in Fig. 1, and a magnified view of the center section is illustrated in Fig. 2. Alloyed ohmic contacts form the source and drain, and rectifying Schottky-contacts form the two gates. The gates are metal stripes, 1 μm wide and 400 μm long, running in parallel between the ohmic contacts. The first gate is separated by 1 μm from the source and by 2 μm from the second gate. Outside the active area,

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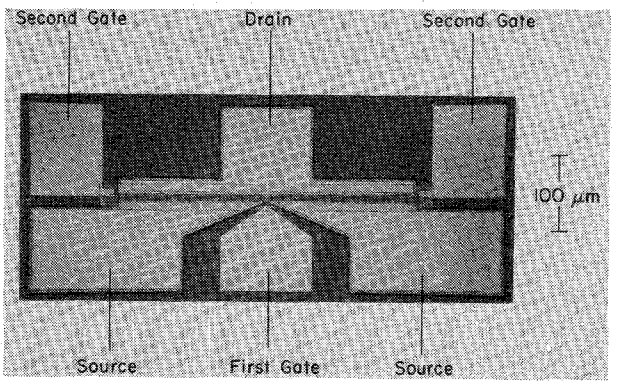


Fig. 1. Microphotograph of the dual-gate MESFET chip.

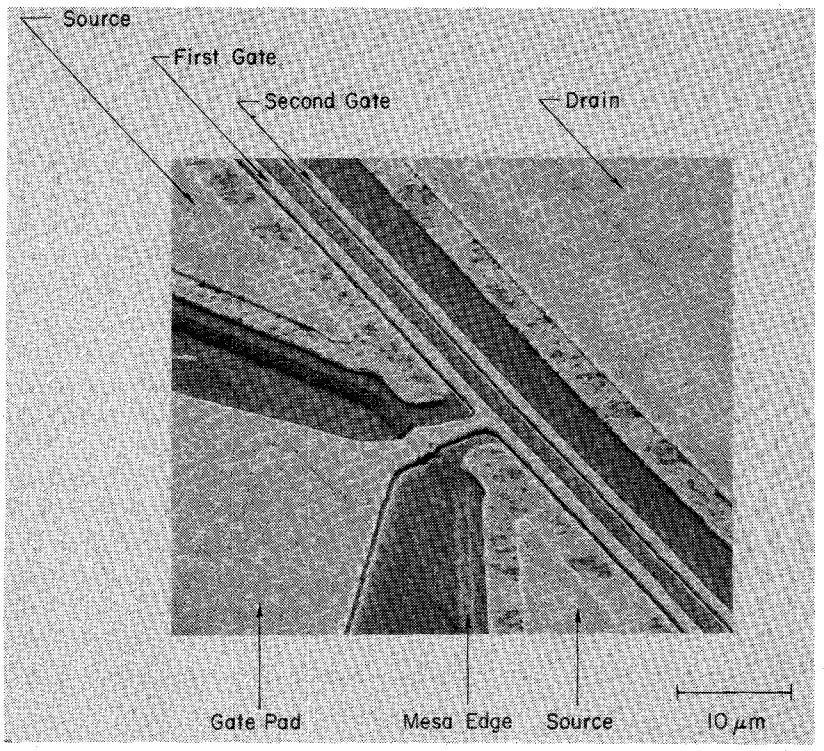


Fig. 2. Scanning-electron micrograph of the dual-gate MESFET's center section.

the epitaxial film is removed by mesa etching. This permits large gate pads to be located on the semi-insulating substrate where they contribute only a small fraction to the interelectrode capacitance.

An artist's concept of the dual-gate MESFET is shown in Fig. 3(a). It is helpful to visualize the device as two separate single-gate MESFET's connected in cascade as shown in Fig. 3(b) [18], [23]. The output current of the first MESFET flows directly into the channel of the second MESFET. If V_{D_1S}, the potential between the two gates, is larger than the threshold voltage for current saturation $V_{D(\text{sat})}$ [Fig. 3(c)], then the first transistor acts essentially as an ideal current source. The bias applied at the second gate V_{G_2S} controls the effective drain voltage V_{D_1S} of the first transistor. V_{D_1S} adjusts to establish the proper gate-to-source bias $V_{G_2S}-V_{D_1S}$ that allows the second transistor to carry the dc current from the first transistor. With positive V_{G_2S} no dc current is flowing into the second gate as long as this voltage stays about 0.5 V below the drain voltage and the first-gate bias is zero or negative ($V_{G_1S} \leq 0$). The model of Fig. 3(b) will frequently be referenced to interpret measured results.

The dual-gate MESFET is characterized as a three-port device with the source as a common terminal. The transistor is measured in a test fixture with drain and gate pads pressed against the center-conductor endings of miniature coaxial lines. The source pads are grounded in this fixture with negligible lead inductance [2]. s-parameters measured at 10 GHz in a 50-Ω system are illustrated in the signal flow graph of Fig. 4. The reference plane for port 1 and port 2 is located at the first gate, and the reference plane for port 3 runs through the center of the

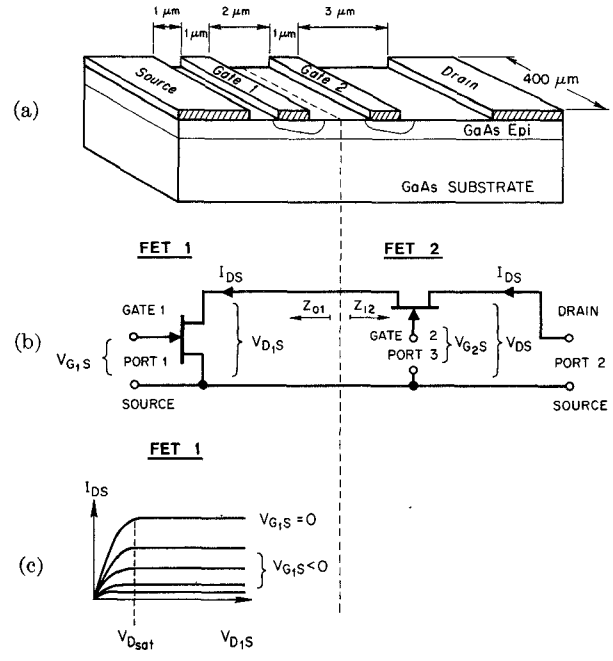


Fig. 3. The dual-gate MESFET is modeled as two single-gate MESFET's connected in cascade. The first MESFET is operated with a common source. Its drain current feeds the source of the second MESFET. The drain current versus drain voltage of the first MESFET is shown in (c).

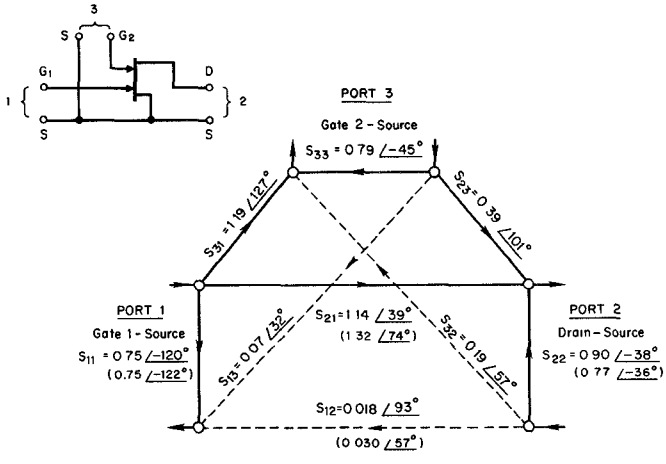


Fig. 4. Three-port signal flow graph of the dual-gate MESFET at 10 GHz. Operating conditions: V_{DS} = 4.5 V; V_{G1S} = 0 V; V_{G2S} = 2.0 V; I_{DSS} = 46 mA; Z_0 = 50 Ω; f = 10 GHz. The s-parameters of a comparable single-gate MESFET are listed in parentheses.

chip perpendicular to the gates. The dc bias has been chosen to yield high gain and allow a simultaneous image match at port 1 and port 2 for a 50-Ω termination at port 3. As expected, strong signal coupling is experienced from gate 1 to drain. But, in addition, nearly the same amount of power is fed from the first gate to the second gate. The reverse couplings are weak, especially s_{12}. The forward coupling from port 3 to port 2 is less pronounced because the output impedance Z_{o1} connected in series with the second-gate capacitance [Fig. 3(b)], keeps the extrinsic transconductance of the second gate low. Z_{o1}, acting also as a series feedback impedance, enhances the reverse signal flow from port 2 to port 3. In comparison, the parameters s_{11}, s_{12}, s_{21}, and s_{22} of a single-gate MESFET with the same geometry are listed in parentheses in Fig. 4. The three-port s-parameters fully describe the dual-gate MESFET's small-signal behavior. They are the basis for computations carried out in the following section.

III. GAIN VERSUS SECOND-GATE TERMINATION

The MESFET characterized as a three-port device is converted to a two-port device by terminating the second gate with an impedance Z_3. The first gate is now considered the input port (port 1) and the drain is considered the output port (port 2). The s-parameters s_{ik}' of this two-port are related to the parameters s_{ik} of the original three-port network by [28]

$$s_{ik}' = s_{ik} + \{(s_{i3} \cdot s_{3k})/[(1/\Gamma_3) - s_{33}]\} \quad (1)$$

where Γ_3 is the reflection coefficient of the load Z_3 with respect to the reference impedance Z_0

$$\Gamma_3 = (Z_3 - Z_0)/(Z_3 + Z_0). \quad (2)$$

Knowing s_{ik}', the maximum available forward gain G_f, and associated reverse isolation, G_r, between the image-matched input and output port can be computed [29]

$$G_f = \left|\frac{s_{21}'}{s_{12}'}\right| [k \mp (k^2 - 1)^{1/2}] \quad (3)$$

and

$$G_r = \left|\frac{s_{12}'}{s_{21}'}\right| [k \mp (k^2 - 1)^{1/2}] \quad (4)$$

with the stability factor k

$$k = \frac{1 + |s_{11}' \cdot s_{22}' - s_{12}' \cdot s_{21}'|^2 - |s_{11}'|^2 - |s_{22}'|^2}{2 \cdot |s_{12}'| \cdot |s_{21}'|}. \quad (5)$$

The negative sign in front of the square root applies if

$$1 - |s_{11}' \cdot s_{22}' - s_{12}' \cdot s_{21}'|^2 + |s_{11}'|^2 - |s_{22}'|^2 > 0. \quad (6)$$

For an RF-shorted second gate, the dual-gate MESFET represents a cascode circuit with a common-source input stage driving a common-gate output stage [Fig. 3(b)]. In Table I, the s-parameters of the dual-gate MESFET with grounded second gate are compared with those of its single-gate counterpart; s_{11}' and $|s_{21}'|$ are practically equal, i.e., the first transistor in Fig. 3(b) essentially determines the input impedance and the magnitude of the forward transfer coefficient s_{21}'. In the dual-gate MESFET, s_{21}' has a smaller phase angle due to the increased electrical length of this device. The magnitudes of s_{12}' and s_{22}' are very different in the two transistors. Signal feedback is considerably reduced, and the output impedance is increased in the dual-gate MESFET. A simple low-frequency ($f < 1$ GHz) analysis of the cascode circuit shows why this is so. A voltage v_{ds}, applied to port 2 in Fig. 3(b), is fed back through the drain–source re-

TABLE I
s-PARAMETERS, FORWARD GAIN, REVERSE ISOLATION, AND STABILITY FACTOR FOR A SINGLE-GATE MESFET AND FOR A DUAL-GATE MESFET WITH RF-GROUNDED SECOND GATE

	s'_{11}	s'_{12}	s'_{21}	s'_{22}	G_f	G_r	k
Dual-Gate MESFET	0.73/-117°	0.011/82°	1.39/44°	0.94/-36°	16 dB	-26 dB	1.7
Single-Gate MESFET	0.75/-122°	0.030/57°	1.32/74°	0.77/-36°	11 dB	-22 dB	2.1

Operating Conditions: Dual-gate MESFET: $V_{DS} = 4.5$ V; $V_{G_1S} = 0$; $V_{G_2S} = 2.0$ V; $I_{DSS} = 46$ mA; $\Gamma_3 = -1$; $f = 10$ GHz. Single-gate MESFET: $V_{DS} = 4.0$ V; $V_{G_1S} = 0$; $I_{DSS} = 56$ mA; $f = 10$ GHz.

sistance of the second MESFET. The resulting drain voltage at the first transistor v_{d_1s} is smaller by the factor μ

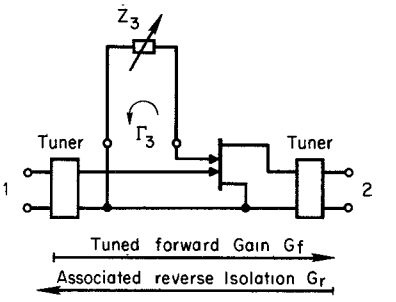
$$\mu = v_{ds}/v_{d_1s} = 2 + g_m R_{ds} \approx 12. \quad (7)$$

R_{ds} is the single-gate output resistance and g_m is the transconductance. Consequently, the voltage fed back to port 1 over the first transistor's drain–gate capacitance is reduced by this factor. The capacitance between drain and gate of the second MESFET does not contribute to feedback because the second gate is RF grounded. The enhancement of the dual-gate MESFET's output impedance is also related to the fact that $v_{d_1s} = v_{ds}/\mu$. At low frequencies, v_{d_1s} causes a drain current at port 2 which is equal to $v_{ds}/(\mu R_{ds})$. The output resistance of the dual-gate MESFET is, therefore, μ times larger than it is in the single-gate version. At high frequencies, the capacitances in the equivalent circuit have also to be considered. As a result, the output resistance starts to fall off at microwave frequencies to a final value equal to the output resistance of a single-gate MESFET.

The contours of constant forward gain G_f and associated reverse isolation G_r have been computed using the s-parameters listed in Fig. 4. They are plotted in the Γ_3 plane in Fig. 5. With the second gate grounded ($\Gamma_3 = -1$), the maximum available forward gain is 16 dB with −26-dB reverse isolation. In comparison, the single-gate MESFET exhibits 11-dB gain with −22-dB isolation (Table I). Up to 21-dB gain can be obtained from the dual-gate MESFET with an inductive termination Z_3. An inductance reduces the reactive mismatch at the input to the channel of the second gate. The reverse isolation decreases, however, and the limits are set by the boundary $k = 1$ beyond which the transistor is potentially unstable. On the other hand, a termination Z_3 can be found that yields forward loss. This happens when the signal flowing via gate 2 to the drain interferes destructively with the signal directly fed from gate 1 to drain.

The frequency dependence of the gain for an RF-grounded second gate is plotted in Fig. 6. Mason's unilateral gain is calculated from the measured s-parameters. The computation yields a 21-dB gain at 10 GHz and a slope of 6 dB per octave.[1] The maximum available gain has been determined with tuned measurements.[2] The gain is 16 dB at 10 GHz and the slope, approximately 5.5 dB/octave. A single-gate MESFET exhibits 11-dB maximum available gain and a slope of 5.5 dB/octave. Below 6 GHz, both MESFET versions are potentially unstable ($k < 1$).[3]

In a practical amplifier application, the second gate does not have to be terminated with a frequency-independent impedance. Moving along the $|\Gamma_3| = 1$ circle in Fig. 5 from an inductive Z_3 to a capacitive Z_3 decreases gain



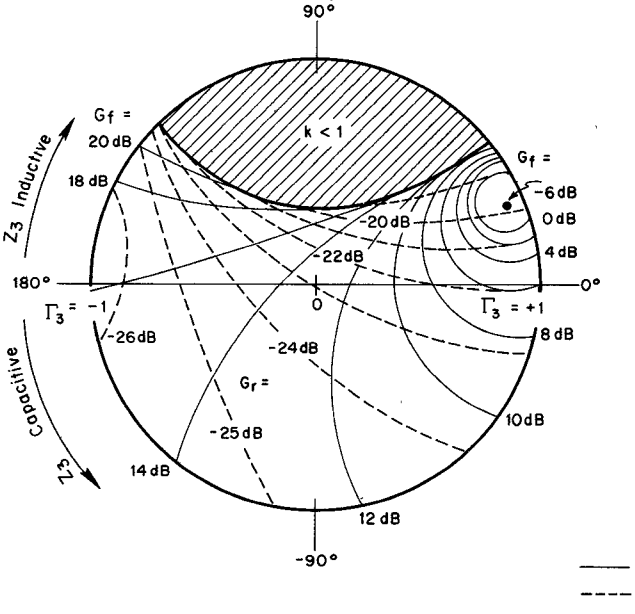


Fig. 5. Tuned forward gain G_f and associated reverse isolation G_r with port 1 as input and port 2 as output port are plotted versus Γ_3 at 10 GHz. Γ_3 is the reflection coefficient of the load impedance Z_3 connected to port 3. In the crosshatched area the transistor is potentially unstable. $V_{DS} = 4.5$ V; $V_{G_1S} = 0$; $V_{G_2S} = 2.0$ V; $Z_0 = 50\ \Omega$; $f = 10$ GHz.

[1] The slope is expected to increase at frequencies above X band.
[2] The measured results agree well with G_f calculated from measured s-parameters according to (3).
[3] That is, both ports cannot be simultaneously image matched. However, stable operation is possible at any frequency, providing that a drain load with a sufficiently large conductance is chosen.

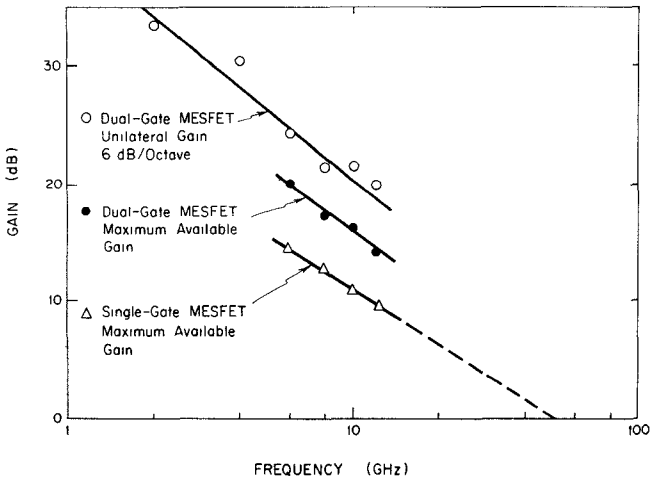


Fig. 6. Calculated unilateral gain and directly measured maximum available gain are plotted versus frequency for a dual-gate MESFET with RF-grounded second gate. $V_{DS} = 4.5$ V; $V_{G_1S} = 0$; $V_{G_2S} = 2$ V; $\Gamma_3 = -1$. The maximum available gain of a single-gate MESFET is shown for comparison.

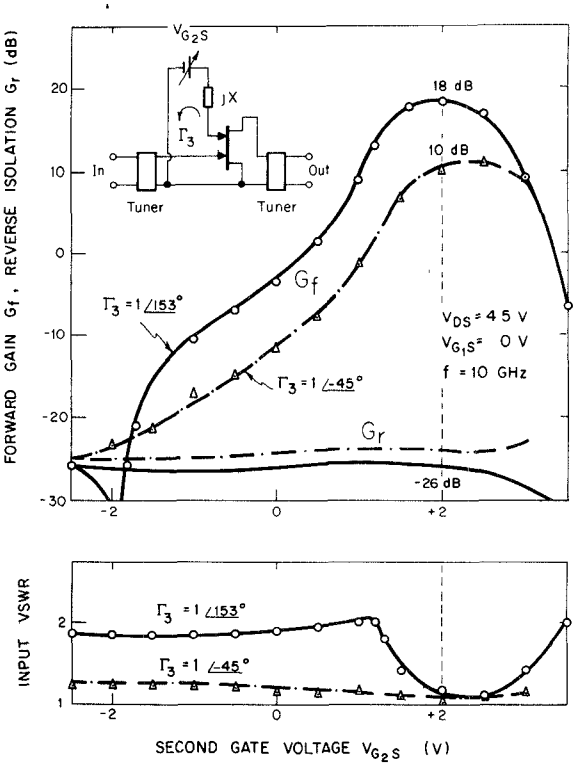


Fig. 7. Forward gain G_f, reverse isolation G_r, and input VSWR versus second gate voltage V_{G_2S} for two reactive terminations at the third port. The first gate and the drain are image matched at $V_{G_2S} = 2.0$ V.

and increases stability. Z_3 as a series-resonant circuit with an appropriate reactance slope could compensate the MESFET's intrinsic gain slope and stabilize the transistor at the lower frequency end ($f < 6$ GHz). In this way, a constant gain with image-matched input and output can be obtained without resorting to resistive feedback [9] or resistive loading of the output coupling network [16].

IV. GAIN MODULATION WITH SECOND-GATE BIAS

Up to this point, device parameters were discussed for fixed dc-bias voltages. In this section, the influence of the second-gate bias V_{G_2S} on forward gain, reverse isolation, input impedance, and transmission phase will be investigated. At 10 GHz, the second-gate termination $\Gamma_3 = 1 \angle 153°$ is chosen, yielding 18-dB gain at $V_{G_2S} = 2.0$ V under image-matched conditions (Fig. 5). The associated reverse isolation is −26 dB. Next, the second-gate voltage is decreased; and the gain, reverse isolation, and input VSWR are measured without readjustment of the tuners. The parameters are plotted in Fig. 7 with solid curves. The forward gain drops from +18 dB to −26 dB. This large gain variation can be explained by referring to the model shown in Fig. 3(b). V_{G_2S} controls the effective drain voltage V_{D_1S} of the first transistor. Decreasing V_{D_1S} increases the output conductance, real $(1/Z_{o1})$, of the first transistor. When this conductance starts to be comparable in magnitude to the input conductance of the second transistor, the transferred RF power begins to decrease. As V_{D_1S} drops below $V_{D(\text{sat})}$, the first transistor acts as an RF voltage-controlled series resistance [Fig. 3(c)]. The RF voltage across this resistance modulates the depletion-layer width under the second gate. By decreasing V_{G_2S}, the dc drain current I_{DS} decreases, and in turn the modulating voltage drop across the series resistance has to decrease. This decrease of the modulating voltage and the decreasing transconductance of the second gate cause the continued gain drop. At −2.5 V, the channel under the second gate is completely depleted and the drain current is cut off. At this voltage, the dual-gate MESFET is a passive, reciprocal device ($G_f = G_r$) in which the drain to first-gate capacitance C_{dg_1} dominates the coupling between the ports. At $V_{G_2S} = -2.0$ V, shortly before the cutoff voltage is reached, the destructive interference of two signals at the output causes a very high forward insertion loss. The two signals result from power coupling over C_{dg_1} in one case and from voltage modulation of the channel current in the other case.

The reverse isolation is −26 dB and remains approximately constant over the entire gate-bias range. The effective drain to first-gate capacitance C_{dg_1} is essentially independent of V_{G_2S}. The same observation was made by Maeda [22]. Also, the input impedance versus V_{G_2S} stays within close limits because the reverse coupling coefficients s_{12} and s_{13} in Fig. 4 remain small in the bias range. The input mismatch plotted in Fig. 7 never rises above 2.1:1.

The forward transmission phase of the dual-gate MESFET is plotted in Fig. 8 versus second-gate voltage. The phase change for a 20-dB gain variation is 75°. If the RF driver is mismatched at $V_{G_2S} = 2$ V, an additional phase change would have to be considered due to the variation of the MESFET's input impedance. In some applications, a phase change of this magnitude is not acceptable. Fortunately, an optimum second-gate termination exists ($\Gamma_3 = 1 \angle -45°$) that minimizes the phase and input-impedance variation. With this Γ_3, a gain variation from its maximum of +10 dB to −10 dB (Fig. 7) changes the phase by only 5° (Fig. 8). The input VSWR reaches a maximum of 1.3:1,

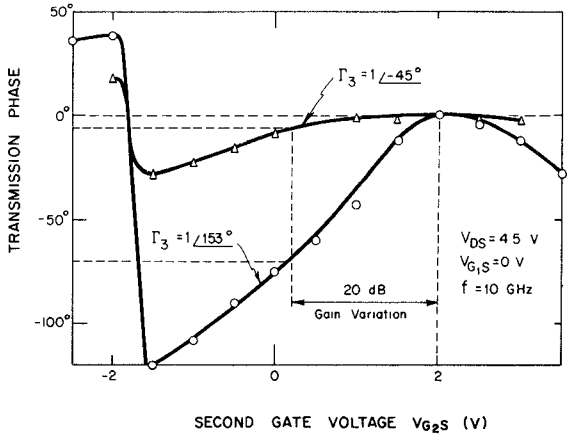


Fig. 8. Transmission phase versus second-gate voltage for two reactive terminations at the third port. The measurement conditions are identical with those in Fig. 7.

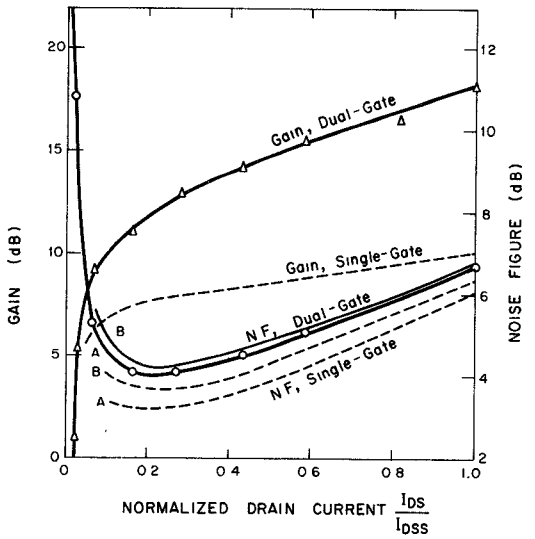


Fig. 9. Minimum noise figure and associated gain versus normalized drain current for single-gate and dual-gate MESFET's. The current is varied by changing the first-gate bias voltage. Curves *A* show the spot noise figure measured on individual transistors. Curves *B* represent calculated noise figures for infinite chains of identical stages. $V_{DS} = 4.5$ V; $V_{G_2S} = 2.0$ V; $\Gamma_3 = 1\angle 141°$; $f = 10$ GHz.

virtually eliminating phase changes due to multiple reflections between the modulator and RF driver. The dual-gate MESFET is, therefore, a modulator with large gain-control range and minimum associated transmission phase change, high unilateral gain, and practically gain-independent input impedance.

V. NOISE PERFORMANCE AND POWER CAPABILITY

The noise figure of a dual-gate MESFET at a fixed frequency is a strong function of the drain current. Therefore, this characteristic is discussed first and compared to the performance of a single-gate MESFET with similar geometry. A second-gate termination is chosen ($\Gamma_3 = 1\angle 141°$) that yields a low noise figure and simultaneously high gain. Fig. 9 illustrates the noise figure and gain performance versus drain current I_{DS}, at 10 GHz. The current is changed by varying the first-gate voltage V_{G1S}. At $V_{G1S} = 0$ the current is I_{DSS}, and the maximum available gain would be 20 dB (Fig. 5). In adjusting the tuner at the MESFET input for minimum noise figure, the gain drops to 18.2 dB yielding a 6.6-dB noise figure. In decreasing the drain current,[4] the noise figure decreases nearly linearly to a minimum of 4.0 dB with 12-dB associated gain. The single-gate MESFET exhibits the same noise figure versus drain-current characteristic (Fig. 9). Its noise-figure minimum is 3.2 dB with 8.0-dB gain.[5] Despite the considerably lower gain of the single-gate MESFET, an infinite chain of cascaded single-gate MESFET's still has a 0.6-dB lower noise figure than a similar chain of dual-gate MESFET's. The difference in noise figure decreases, however, if the loss in the input matching and interstage coupling is considered.

In a dual-gate MESFET, the noise-figure minimum can be approached only if the output of the first transistor is noise-matched to the input of the second transistor [Fig. 3(b)]. The input impedance Z_{i2} can be adjusted by varying the external impedance Z_3. On the other side, the output impedance of the first transistor Z_{o1} can be varied with the potential V_{D_1S}. This potential is controlled by the second-gate bias. In Fig. 10, the noise figure and gain are plotted versus V_{G_2S}. The noise figure reaches its minimum at 2 V. By decreasing V_{G_2S}, it rises, first slowly, and then, below 0.5 V, very rapidly. It is known that the noise figure of single-gate MESFET's is very insensitive to the drain voltage as long as V_{D_1S} is above $V_{D(sat)}$ [Fig. 3(c)], [5], [6]. Therefore, it is assumed that the noise figure of the first transistor in Fig. 3(b) stays constant for $V_{G_2S} > 0.5$ V, and the gain and overall noise-figure variation is solely due to the change in the output conductance of the first stage. This conductance in turn determines the impedance mismatch between the stages and the noise power generated by the second transistor.

Van der Ziel proposed to improve the noise figure of dual-gate FET's by neutralizing the drain-to-gate capacitance of the first transistor in Fig. 3(b) and by providing a tuned matching network between the two transistors [30]. To make this improvement possible, an ohmic contact between the two gates, a neutralization circuit, a tuning reactance to ground, and dc-blocking capacitors are proposed in addition to the RF-grounding and dc-biasing circuit at the second gate. The realization of this is a rather demanding task at *X* band. Asai's technique to improve the dual-gate noise figure requires a longer second gate and thicker second channel [17], [18]. This approach still needs theoretical justification. For device fabrication, a critical second alignment step is required

[4] The tuning was optimized at each drain current.

[5] The compared single-gate MESFET has not been fabricated on the same chip. However, its gate length, gate-to-source spacing, channel thickness, and epitaxial material characteristics closely match the dual-gate MESFET's parameters.

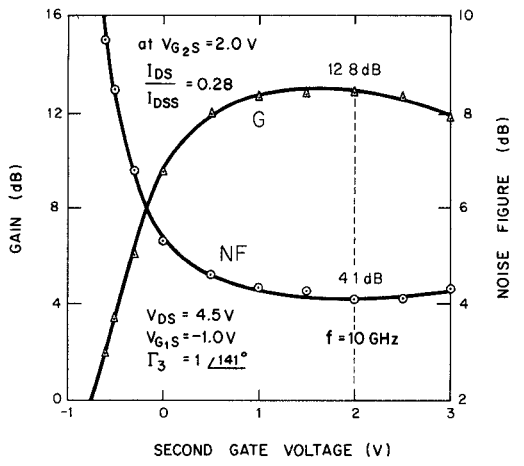


Fig. 10. Minimum noise figure and associated gain versus second-gate voltage.

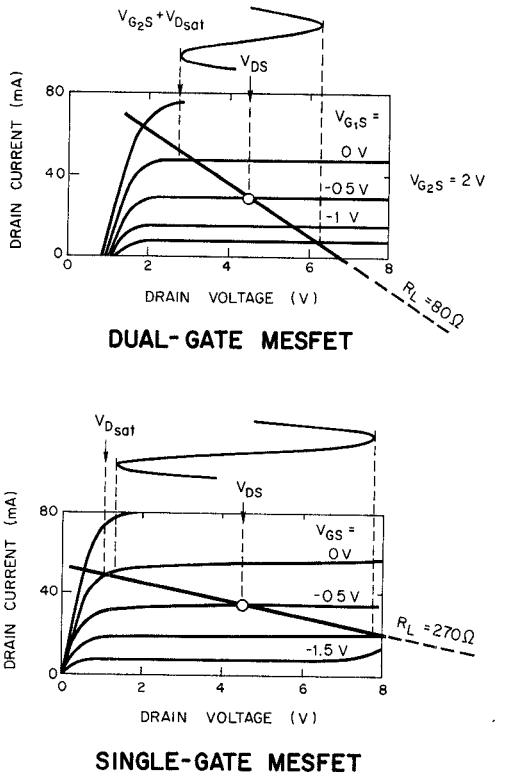


Fig. 11. Static drain-current versus drain-voltage characteristics, dc bias points, and load lines for the two MESFET versions. The MESFET's are operated with identical dc bias, power consumption, and small-signal gain. The maximum drain-voltage swing for "linear" operation is illustrated.

which raises the cost of the dual-gate over the single-gate MESFET. In contrast, it is demonstrated here that an optimized second-gate termination and second-gate dc bias yield a dual-gate noise figure of 4.0 dB at 10 GHz, only 0.8 dB above the minimum noise figure of the compared single-gate MESFET.

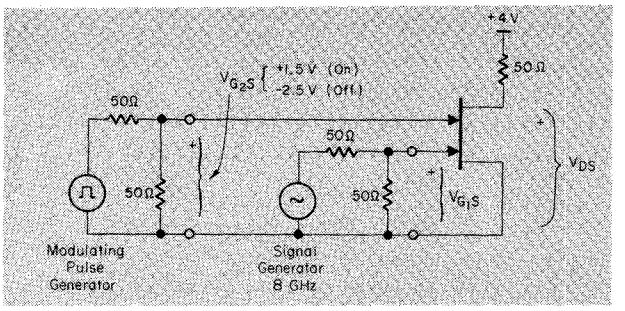
After comparing the noise characteristics, the power capability of the two MESFET versions are discussed. For this purpose, a single-gate and a dual-gate MESFET with approximately equal gate width and drain current I_{DSS} are chosen. Both transistors are operated at the same drain and gate bias (V_{DS} = 4.5 V, $V_{G_1S} = V_{GS} = -0.5$ V) with about equal dc power dissipation (130 mW). In addition, the two MESFET's are operated at the same small-signal gain, i.e., they both yield 9-dB gain at 10 GHz. The single-gate MESFET is image matched at both ports. For the dual-gate MESFET, the input is image matched, the output capacitance is parallel resonated, and the load resistance is adjusted for equal gain (R_L = 80 Ω). The second gate is terminated with $\Gamma_3 = 1 \angle 153°$ and biased to V_{G_2S} = 2.0 V. The resulting output power for 1-dB gain compression is +9 dBm for the single-gate and +10 dBm for the dual-gate MESFET.

Under the stated conditions, both MESFET's have about the same power capability. The drive conditions are illustrated in Fig. 11. The static drain-current versus drain-voltage characteristics, the dc bias points, and the load lines of the two MESFET's are shown. For the dual-gate MESFET, the maximum drain-voltage swing is limited by $V_{DS} - (V_{G_2S} + V_{D(sat)})$. If V_{DS} drops below $V_{G_2S} + V_{D(sat)}$, the second transistor in the model of Fig. 3(b) is driven into the resistive region which raises the drain to second-gate capacitance more than an order of magnitude. The output is now shunted by the second-gate termination which drastically decreases the RF output impedance. If V_{DS} is reduced below V_{G_2S}, the second gate is sufficiently forward biased to draw dc current. In the single-gate version, the maximum drain-voltage swing is larger since it is limited only by $V_{DS} - V_{D(sat)}$. For equal gain performance, however, the load resistance R_L must be considerably higher.[6] The larger R_L offsets the advantage of the larger voltage swing $\hat{v}_{ds}$ because the delivered RF power is proportional to $\hat{v}_{ds}^2/R_L$.

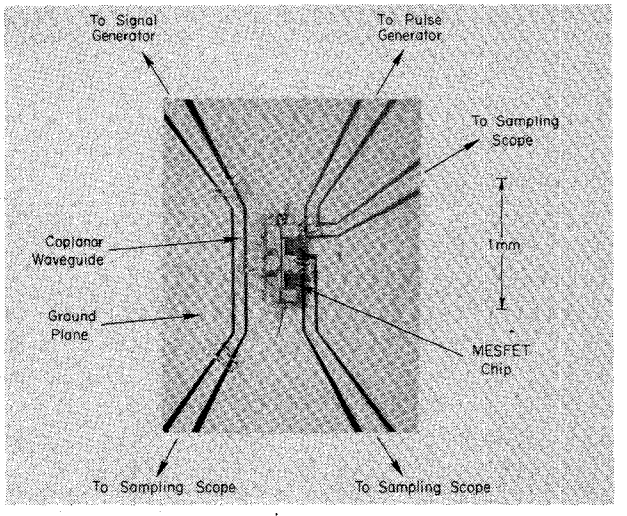
VI. HIGH-SPEED AMPLITUDE MODULATION OF AN RF CARRIER

The dual-gate MESFET as a modulator offers a very fast switching response. This capability is demonstrated here by pulse-amplitude modulating a microwave carrier. The basic test circuit is illustrated in Fig. 12(a). The output of an 8-GHz signal generator is fed directly into the first gate without impedance transformation. A pulse generator switches the second gate between −2.5 V (off) and +1.5 V (on). This pulse is synchronized with the 8-GHz signal, so the resulting RF burst can be observed on a sampling scope. The drain and the two gates are connected to 50-Ω output lines in order to compare the three waveforms simultaneously on the sampling scope. The physical arrangement of the test circuit in the vicinity of the MESFET chip is shown in Fig. 12(b). The transmission

[6] The load resistance is 270 Ω. The ratio of the two load resistances would be four if the dual-gate MESFET had the same equivalent circuit (with no feedback elements) as its single-gate counterpart with the exception of a negligibly small output conductance.



(a)



(b)

Fig. 12. Pulsed-amplitude modulation of an 8-GHz carrier with the dual-gate MESFET. (a) Illustrates the basic test circuit. (b) Shows the arrangement of the 50-Ω coplanar transmission lines on a sapphire substrate in the vicinity of the MESFET chip.

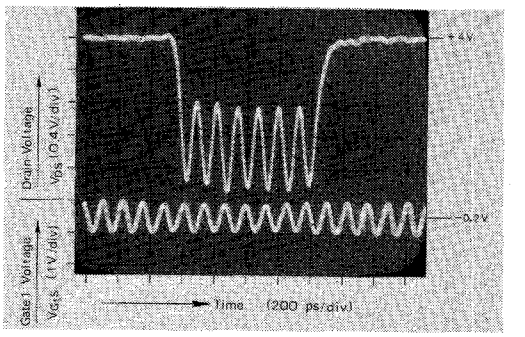


Fig. 13. Pulsed-amplitude modulation of an 8-GHz carrier. The RF input voltage at the first gate is shown in the lower trace and the output-voltage waveform at the drain is shown in the upper trace.

lines are 50-Ω coplanar waveguides [31] on a sapphire substrate. The coplanar lines are tapered from a size convenient for connector mating close to the substrate edge to a size suitable for short wire bonds to the chip [32]. The coplanar waveguide also has the advantage of a continuous ground plane on the substrate surface, so that low-inductance grounding of the MESFET source can be achieved.

The voltage waveforms are shown in the oscilloscope display of Fig. 13. On the horizontal time axis, the scale is 200 ps/div. The sinusoidal waveform at the bottom is the 8-GHz signal voltage that is applied to the first gate. The drain voltage is shown in the upper trace. As long as the second-gate voltage is low, the MESFET is turned off; the output potential is at the supply voltage, and no RF signal is coupled to the output. When the second-gate voltage is pulsed to a positive potential, the MESFET is switched on; drain current flows causing a voltage drop in the 50-Ω load resistor. The MESFET transmits the RF input signal. The RF burst is about 7 cycles long and full switching is accomplished in less than one RF cycle. With the RF signal turned off, a drain-voltage fall time of 65 ps and rise time of 100 ps is measured. This compares with a 100-ps rise time and 125-ps fall time of the modulating pulse. Only a fraction of the applied voltage swing drives the MESFET through its active region which results in the slightly faster output-switching response. The switching speed in this experiment is limited by the pulse generator and not by the MESFET. It demonstrates the MESFET's capability to switch from gain to high insertion loss within approximately one RF cycle at X-band frequencies.

VII. CONCLUSIONS

The GaAs MESFET with two 1-μm Schottky-barrier gates and an inductive second-gate termination exhibits 18-dB stable gain at 10 GHz. This compares with 11-dB maximum available gain for the single-gate counterpart. The minimum noise figure is 4.0 dB with 12-dB associated gain as opposed to a 3.2-dB noise figure and 8.0-dB gain in the single-gate version. The output impedance of the dual-gate MESFET is, in general, higher and dependent on the second-gate termination. Both MESFET versions deliver approximately 10-mW output power at 1-dB gain compression if they are operated with identical dc bias, power consumption, and small-signal gain. The dual-gate version offers the added feature of gain modulation with 44-dB gain control and less than 70-ps modulating response time.

The application potential of the single-gate versus dual-gate MESFET in small-signal amplifiers can now be clearly outlined. The signal-gate MESFET has a slightly lower noise measure. If the lowest possible amplifier noise figure is required, then the single-gate version has to be used in the first stage. However, for all the other stages, the dual-gate version has definite advantages. First, it yields higher gain, thereby reducing the number of required stages and the cost of an amplifier. Second, it enables automatic gain control over a large dynamic range with minimum transmission phase shift. Third, it allows gain-slope compensation and low-frequency stabilization with a simple series-resonant circuit between second gate and source.

The dual-gate MESFET is also a modulator with a high on-to-off gain ratio, practically gain-independent input impedance, and ultrafast switching speed. These features make the device very attractive for subnanosecond pulsed-amplitude modulation (PAM). They are also very useful in applications requiring phase- or frequency-shift keyed carrier modulation (PSK) and (FSK). Biphase modula-

tion, for example, can be easily realized by operating two dual-gate MESFET's in parallel with a common drain output. The 0°- and 180°- shifted carriers are fed to the first gates and complimentary modulating pulses are applied to the second gates. The capability of performing multiple functions opens a wide basis for innovations in the application of the dual-gate MESFET in microwave systems.

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